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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/687,124	10/16/2003	Richard E. Fackenthal	ITL.1046US (P17448)	7345

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TROP PRUNER & HU, PC
1616 S. VOSS ROAD, SUITE 750
HOUSTON, TX 77057-2631

EXAMINER	
LAMARRE, GUY J	

ART UNIT	PAPER NUMBER
2133	

DATE MAILED: 06/08/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/687,124	FACKENTHAL, RICHARD E.	
	Examiner	Art Unit	
	Guy J. Lamarre	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 October 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-48* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-48* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 October 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *10/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

* Pursuant to 35 USC 131, **Claims 1-48 are** presented for examination.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-48 are rejected under 35 U.S.C. 102 (b) as being anticipated by **Gregoti et al.** '*Construction of Polyvalent Error Control Codes for Multilevel Memories,*' IEEE, 2000, pp751-754, (IDS of 10/2003).

As per Claims 1-48, Gregoti et al. discloses, in Figs. 1-3 and related description, equivalent data storing along with equivalent error control comprising selectively storing data in a memory array at different densities per cell; and implementing error correction depending on the density of data storage, e.g., in Fig. 3 wherein ECC (e.g., page 752) level is selectively enabled based on desired cell density (e.g., Fig. 1) level at page 754 col. 2 para. 1.

As per Claim 1, **Gregoti** et al. discloses, in Figs. 1-3 and related description, equivalent method comprising: selectively storing data in a memory array at different densities per cell; and implementing error correction depending on the density of data storage.
As per Claim 2, **Gregoti** et al. discloses, in Figs. 1-3 and related description, equivalent method of claim 1 including selectively storing data in a memory at different densities per cell by using different numbers of threshold voltage levels in a given cell.
As per Claim 3, **Gregoti** et al. discloses, in Figs. 1-3 and related description, equivalent method of claim 2 including using a higher density mode with double the number of threshold levels as a lower density mode.

As per Claim 4, Gregoti et al. discloses, in Figs. 1-3 and related description, equivalent method of claim 3 including using a higher density mode with four threshold levels and a lower density mode using two threshold levels.

As per Claim 5, Gregoti et al. discloses, in Figs. 1-3 and related description, equivalent method of claim 1 wherein implementing error correction code depending on the density of data storage includes determining whether data is in a higher or lower density mode and if the data is in a higher density mode, implementing error correction code and if the data is in a lower density mode, omitting error correction code.

As per Claim 6, Gregoti et al. discloses, in Figs. 1-3 and related description, equivalent method of claim 5 including using a flag to indicate whether or not the data is in a lower or higher density mode.

As per Claim 7, Gregoti et al. discloses, in Figs. 1-3 and related description, equivalent method of claim 5 including allowing overwriting when the data is stored in the lower density mode.

As per Claim 8, Gregoti et al. discloses, in Figs. 1-3 and related description, equivalent method of claim 7 including preventing overwriting when the data is stored in the higher density mode.

As per Claim 9, Gregoti et al. discloses, in Figs. 1-3 and related description, equivalent method of claim 1 including allowing overwriting of stored data when error correcting codes are not provided for that data.

As per Claim 10, Gregoti et al. discloses, in Figs. 1-3 and related description, equivalent method of claim 1 including providing a multi-level memory cell array having a capacity of at least four levels.

As per Claim 11, Gregoti et al. discloses, in Figs. 1-3 and related description, equivalent

method of claim 10 including using at least two bits to represent said at least four levels.

As per Claim 12, **Gregoti** et al. discloses, in Figs. 1-3 and related description, equivalent method of claim 11 including using one of said bits as a more significant bit and the other of said bits as a less significant bit.

As per Claim 13, **Gregoti** et al. discloses, in Figs. 1-3 and related description, equivalent method of claim 12 wherein data from at least two cells forms a codeword and grouping the more significant bits from different cells together.

As per Claim 14, **Gregoti** et al. discloses, in Figs. 1-3 and related description, equivalent method of claim 13 including providing more significant bits in one half of a word and less significant bits in the other half of a word.

As per Claim 15, **Gregoti** et al. discloses, in Figs. 1-3 and related description, equivalent article comprising a medium storing instructions that, if executed, enable a processor-based system to: selectively store data in a memory array at different densities per cell; and implement error correction depending on the density of data storage.

As per Claim 16, **Gregoti** et al. discloses, in Figs. 1-3 and related description, equivalent article of claim 15 further storing instructions that, if executed, enable the system to selectively store data in a memory at different densities per cell by using different numbers of threshold voltage levels in a given cell.

As per Claim 17, **Gregoti** et al. discloses, in Figs. 1-3 and related description, equivalent article of claim 16 further storing instructions that, if executed, enable the system to use a higher density mode with double the number of threshold levels as a lower density mode.

As per Claim 18, **Gregoti** et al. discloses, in Figs. 1-3 and related description, equivalent article of claim 17 further storing instructions that, if executed, enable the system to use a higher density mode with four threshold levels and a lower density mode using two threshold levels.

As per Claim 19, **Gregoti** et al. discloses, in Figs. 1-3 and related description, equivalent article of claim 15 further storing instructions that, if executed, enable the system to determine whether data is in a higher or lower density mode and if the data is in a higher density mode, implement error correction code and if the data is in a lower density mode, omit error correction code.

As per Claim 20, **Gregoti** et al. discloses, in Figs. 1-3 and related description, equivalent article of claim 19 further storing instructions that, if executed, enable the system to use a flag to indicate whether or not the data is in a lower or higher density mode.

As per Claim 21, **Gregoti** et al. discloses, in Figs. 1-3 and related description, equivalent article of claim 19 further storing instructions that, if executed, enable the system to allow overwriting when the data is stored in a higher density mode.

As per Claim 22, **Gregoti** et al. discloses, in Figs. 1-3 and related description, equivalent article of claim 20 further storing instructions that, if executed, enable the system to prevent overwriting when data is stored in the higher density mode.

As per Claim 23, **Gregoti** et al. discloses, in Figs. 1-3 and related description, equivalent article of claim 15 further storing instructions that, if executed, enable the system to allow overwriting of stored data when error correcting codes are not provided for that data.

As per Claim 24, **Gregoti** et al. discloses, in Figs. 1-3 and related description, equivalent article of claim 15 further storing instructions that, if executed, enable the system to provide a multi-level memory cell array having a capacity of at least four levels.

As per Claim 25, **Gregoti** et al. discloses, in Figs. 1-3 and related description, equivalent article of claim 24 further storing instructions that, if executed, enable the system to use at least two bits to represent said at least four levels.

As per Claim 26, **Gregoti** et al. discloses, in Figs. 1-3 and related description, equivalent article of claim 25 further storing instructions that, if executed, enable the system to use one of said bits as a more significant bit and the other of said bits as a less significant bit.

As per Claim 27, **Gregoti** et al. discloses, in Figs. 1-3 and related description, equivalent article of claim 26 wherein data from at least two cells forms a codeword and further storing instructions that, if executed, enable the system to group the more significant bits from different cells together.

As per Claim 28, **Gregoti** et al. discloses, in Figs. 1-3 and related description, equivalent article of claim 27 further storing instructions that, if executed, enable the system to provide more significant bits in one half of a codeword and less significant bits in the other half of a codeword.

As per Claim 29, **Gregoti** et al. discloses, in Figs. 1-3 and related description, equivalent memory comprising: a memory array; and a controller coupled to said memory array to selectively store data in the memory array at different densities per cell and to implement error correction depending on the density of data storage.

As per Claim 30, **Gregoti** et al. discloses, in Figs. 1-3 and related description, equivalent memory of claim 29 wherein said memory array is a multi-level flash memory array.

As per Claim 31, **Gregoti** et al. discloses, in Figs. 1-3 and related description, equivalent memory of claim 29 wherein said controller to determine whether data is in a higher or lower density mode and if the data is in a higher density mode, implement error correction and if the data is in a lower density mode, omit error correction.

As per Claim 32, **Gregoti** et al. discloses, in Figs. 1-3 and related description, equivalent memory of claim 31 said controller to allow overwriting when the data is stored in the lower density mode.

As per Claim 33, **Gregoti** et al. discloses, in Figs. 1-3 and related description, equivalent memory of claim 32 said controller to prevent overwriting when the data is stored in the higher density mode.

As per Claim 34, **Gregoti** et al. discloses, in Figs. 1-3 and related description, equivalent memory of claim 29 said controller to allow overwriting of stored data when error correcting code is not provided for that data.

As per Claim 35, **Gregoti** et al. discloses, in Figs. 1-3 and related description, equivalent memory of claim 29 said controller to use at least two bits to represent four threshold voltage levels.

As per Claim 36, **Gregoti** et al. discloses, in Figs. 1-3 and related description, equivalent memory of claim 35 said controller to use one of said bits as a more significant bit and the other of said bits as a less significant bit.

As per Claim 37, **Gregoti** et al. discloses, in Figs. 1-3 and related description, equivalent memory of claim 36 said controller to group the more significant bits from different cells together.

As per Claim 38, **Gregoti** et al. discloses, in Figs. 1-3 and related description, equivalent system comprising: a processor; a wireless interface; a memory coupled to said processor; and a controller coupled to said memory to selectively store data in said memory at different densities per cell and to implement error correction depending on a density of data storage.

As per Claim 39, **Gregoti** et al. discloses, in Figs. 1-3 and related description, equivalent system of claim 38 wherein said memory is a multi-level flash memory.

As per Claim 40, **Gregoti** et al. discloses, in Figs. 1-3 and related description, equivalent system of claim 38 wherein said controller to determine whether data is in higher or lower density mode and if the data is in a higher density mode, implement error correction and if the

data is in a lower density mode, omit error correction.

As per Claim 41, **Gregoti** et al. discloses, in Figs. 1-3 and related description, equivalent system of claim 40 said controller to allow overwriting when the data is stored in the lower density mode.

As per Claim 42, **Gregoti** et al. discloses, in Figs. 1-3 and related description, equivalent system of claim 41 said controller to prevent overwriting when the data is stored in the higher density mode.

As per Claim 43, **Gregoti** et al. discloses, in Figs. 1-3 and related description, equivalent system of claim 38 said controller to allow overwriting of stored when error correcting codes are not provided for that data.

As per Claim 44, **Gregoti** et al. discloses, in Figs. 1-3 and related description, equivalent system of claim 38 said controller to use at least two bits to represent four threshold levels.

As per Claim 45, **Gregoti** et al. discloses, in Figs. 1-3 and related description, equivalent system of claim 44 said controller to use one of said bits as a more significant bit and the other said bits as a less significant bit.

As per Claim 46, **Gregoti** et al. discloses, in Figs. 1-3 and related description, equivalent system of claim 45 said controller to group the more significant bits from different cells together.

As per Claim 47, **Gregoti** et al. discloses, in Figs. 1-3 and related description, equivalent system of claim 38 wherein said wireless interface includes an antenna.

As per Claim 48, **Gregoti** et al. discloses, in Figs. 1-3 and related description, equivalent system of claim 47 wherein said wireless interface includes a dipole antenna.

CONCLUSION

* Any response to this action should be mailed to:

Commissioner of Patents and Trademarks, Washington, D.C. 20231

or faxed to: (571) 273-8300 for all formal communications.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Guy J. Lamarre, P.E., whose telephone number is (571) 272-3826. The examiner can normally be reached on Monday to Friday from 9:30 AM to 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert De Cady, can be reached at (571) 272-3819.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (571) 272-3609.

Information regarding the status of an application may also be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Guy J. Lamarre, P.E
Primary Examiner